

# Distilling Sparse Linear Algebra

Aleksey Tyurin<sup>1,2</sup>

alekseytyurinspb@gmail.com <sup>1</sup>JetBrains Research, Russia <sup>2</sup>St. Petersburg University, Russia



Fusion is an ubiquitous optimization for dence applications widely used, e.g., in Tensorflow, aimed to reduce memory usage. Is is also a highly desired optimization in sparse applications [1] but it is hard to implement due to pointer-chaising [2] nature of the latter. The basics of this optimization is the removal of *intermediate* data structures : those which are firstly constructed and then deconstructed. This is common for functional programming where such optimization is often addressed as *deforestation*.

We propose the usage of a functional quad-tree representation for sparse data and *disillation* to support fusion for sparse applications.



Distillation implements deforestation by removing intermediate data structures, i.e. those first constructed and then deconstructed, providing the following bonuses

- Specialization, i.e., it partially evaluates the program on statically known arguments.
- Yields *tail recursive modulo cons* programs, which could ease the following translation to hardware.
- Gives potentially asymptotically greater speed-up than deforestation.



#### Motivation: Kernel fusion



Motivation: Mask fusion [1]



Fused masking requires 8 reads and writes to matrix applying mask ahead-of-time

## **Evaluation:** Hardware



# **Evaluation:** Software



# Implementation

- We use the distiller authored by Geoff Hamilton [3] and its functional language to evaluate the approach in terms of *reductions* and *mem*ory accesses.

### Results

- Distillation gives prominent results namely
- Shows up to 60% less reductions and 45%less memory accesses in software.

# **Future Research**

- Moving the disiller from proof-of-concept to ready-to-use.
- Moving the hardware compiler from proof-ofconcept to ready-to-use.

In order to provide both enough performance and interoperability with C++ (in which modern sparse frameworks are mostly written) we aim to synthesize a FPGA kernel from distilled functional program and utilize FHW project [4] to do so.

- Shows up to 20% less clock cycles and memory writes in hardware.
- Bridge the gap between our approach and existing sparse frameworks in a form of OpenCL-like kernels.
- Real-world examples evaluation.

#### References

#### Contact Us

Our team:

- Aleksey Tyurin: alekseytyurinspb@gmail.com
- Daniil Berezun: daniil.berezun@jetbrains.com
- Ekaterina Vinnik: catherine.vinnik@gmail.com
- Semyon Grigorev: s.v.grigoriev@spbu.ru
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